

December 2, 2022

Hon. Nathanael M. Cousins
San Jose Courthouse, Courtroom 5 - 4th Floor
280 South 1st Street, San Jose, CA 95113

Re: ***VLSI Technology LLC v. Intel Corporation***, Case No. 5:17-cv-05671-BLF (N.D. Cal.)

Dear Judge Cousins:

The parties request the Court's assistance to resolve the dispute presented below.

Intel's Position

On October 25, 2018, the Court ordered VLSI to supplement its PLR 3-8 Damages Contentions to explain how the payments set forth in patent agreements VLSI had identified support VLSI's multi-billion dollar damages assertion. D.I. 172 ("Order") at ¶ 5. VLSI has failed to comply with this Order. Although Intel has given VLSI four opportunities to supplement its contentions, VLSI still has not connected any patent agreements to its extraordinary \$5.4 billion damages demand. It appears that VLSI will instead attempt to spring its theory on Intel late in the case. VLSI should not be permitted to do so. As a result of VLSI's violation of the Court's Order despite numerous opportunities over a period of years to comply, Intel moves to strike from VLSI's damages contentions any reliance on patent agreements and requests an order precluding VLSI from relying on any patent agreements in this case.

The Court Ordered VLSI to Explain How Any Patent Agreements Support Its Damages Number

In its initial damages contentions served on June 21, 2018, VLSI claimed \$2.6 billion to \$5.4 billion in damages. As Intel explained in its September 19, 2018 motion to compel and during the October 24, 2018 hearing on the motion, VLSI's contentions provide no plausible theory to support this unreasonable number. D.I. 152. The Court granted Intel's motion and ruled that if VLSI intends to rely on patent agreements to support its damages claim, VLSI had to disclose in its PLR 3-8 contentions: "(i) the identity of the specific agreements on which VLSI relies; (ii) ***an explanation of how the payments set forth in the agreements support VLSI's damages claim***; and (iii) ***an explanation of VLSI's bases for contending that the agreements are comparable to a hypothetical license to the asserted patents***." D.I. 172 (emphasis added).

VLSI Has Failed to Comply with the Court's Order

VLSI supplemented its damages contentions four times since the October 2018 Order—on December 12, 2018, January 14, 2019, October 27, 2021, and September 12, 2022. Its damages range has become even more unreasonable, and is now \$5.3 billion to \$5.4 billion. Despite seeking these unprecedented damages, VLSI continues to disregard the Court's Order:

- VLSI has identified eight Intel litigation settlement agreements—agreements with DEC, Intergraph, WARF, [REDACTED], Nvidia, [REDACTED] Transmeta, and MicroUnity—but ***has not explained how any agreement is connected to its \$5.4 billion damages number***. VLSI 4th Suppl. Damages Contentions ("4th Contentions") 80-94. None of these agreements has a payment amount anywhere close to \$5.4 billion—instead, the amounts are billions of dollars lower. VLSI has not set forth any explanation—no math, formula, or theory—as to how any agreement supports its damages number.

- VLSI does not attempt to set forth a basis for contending that any of the DEC, Intergraph, [REDACTED], Nvidia, [REDACTED] or Transmeta agreements is technologically or economically comparable to a hypothetical license to the asserted patents. It asserts only that these agreements are “*potentially* comparable” and it “*may*” later rely on them. *Id.* at 91.
- VLSI asserts that its experts “*may consider*” “other” unidentified agreements. *Id.* at 80. VLSI has not set forth the payment amounts of any of these “other” agreements, or attempted to explain how those amounts could possibly support its \$5.4 billion demand.¹

As a result, nearly four years after the Court’s Order, VLSI *still* has not explained how any patent agreement could possibly support its damages demand. This has significantly prejudiced Intel. The purpose of PLR 3-8 is to allow the defendant to know at the outset of the case how the plaintiff will argue that patent agreements are used to determine its damages number. *Twilio, Inc. v. Telesign Corp.*, 2017 WL 5525929, at *2 (N.D. Cal. Nov. 17, 2017). This allows the defendant to test and challenge the theory, develop its own evidence in rebuttal, take discovery relevant to the theory, and prepare its rebuttal expert arguments. Intel has been precluded from doing this with respect to any theory regarding the Intel litigation settlements.

It is too late for VLSI to fix this prejudice now. Four years is enough opportunity for VLSI to comply. Under PLR 3-8, Intel should have had the full discovery period to test and rebut VLSI’s arguments. Even if VLSI complied with the Court’s Order today, Intel was precluded for years from taking discovery on how any agreement could support VLSI’s multi-billion dollar damages claim—including written discovery, depositions, additional document production, and third party discovery and depositions (which could take months to arrange and complete). Intel also has been developing expert arguments for months—it should not be forced to re-do that work if VLSI now decides to comply with the Court’s Order from 2018. Indeed, this is precisely the type of prejudice that PLR 3-8 was designed to avoid.

VLSI argues that its latest supplement fixes the flaws in its contentions. VLSI is wrong.

- VLSI asserts that it need not provide any further information for the DEC, Intergraph, [REDACTED], Nvidia, [REDACTED] or Transmeta agreements because it will use the agreements only “*in rebuttal*” to Intel’s damages arguments. 4th Contentions 80-91. But the Court’s Order contains no such exception. VLSI has the burden on damages and under PLR 3-8 was required to disclose at the start of the case how any agreements it will rely on are comparable and allegedly support its damages number. If a party could avoid disclosure of “rebuttal” evidence, PLR 3-8 would be meaningless—plaintiffs could entirely avoid the disclosure requirements simply by asserting they intend to use agreements in “rebuttal.” Further, as a matter of Federal Circuit law, VLSI cannot rely on agreements for any purpose—“rebuttal” or otherwise—without showing the agreements are comparable to a license to the asserted patents. *Lucent Techs., Inc. v. Gateway, Inc.*, 580 F.3d 1301, 1325-32 (Fed. Cir. 2009). And that is the problem—VLSI has failed to provide *any basis* to allege that these settlements are technologically or economically comparable.²

¹ VLSI asserts that it may later “re-assert” “I²C” agreements that it dropped from its contentions. 4th Contentions 80 n.3. This would violate the Court’s Order and should not be allowed.

² The *Tela* case that VLSI cites does not hold otherwise. That court did not allow the use of *non-comparable* agreements to rebut an opinion on *comparable agreements* as VLSI proposes to do.

- VLSI argues that it will affirmatively rely on just the MicroUnity and WARF settlements to support its damages demand. 4th Contentions 80-91. But VLSI *still* does not explain how the payments amounts in these agreements could possibly support its \$5.4 billion demand. Neither agreement has a payment anywhere close to VLSI's number. In fact, the payments are *more than \$5 billion lower* than VLSI's number.
- VLSI does not connect the MicroUnity or WARF settlements to its damages numbers on a "per-patent" basis, as it incorrectly asserts below. ***VLSI does not provide a damages number based on these settlements for any of the asserted patents.*** VLSI mentions the '836 patent below, but the only "per patent" numbers VLSI provides for that patent—using other methodologies unrelated to comparable agreements—are at least *5 times lower* than the amounts in the MicroUnity and WARF settlements. VLSI also never explains how the payments in these settlements—which span a range of nearly \$200 million—could possibly support a specific number. VLSI apparently seeks to use these settlements simply to put large amounts before the jury to try to make its damages claim seem less extreme.

The time for VLSI to comply with the Court's Order has passed. Intel respectfully moves to strike from VLSI's damages contentions any reliance on patent agreements, including the Intel litigation settlements, and requests an order precluding VLSI from relying on patent agreements in this case. *See Shared Memory Graphics LLC v. Apple Inc.*, 2011 WL 3878388, at *4, *8 (N.D. Cal. Sept. 2, 2011) (striking amended infringement contentions that failed to correct deficiencies identified in prior order compelling amended contentions).

VLSI's Position

Intel's motion omits facts about this case's history that undercut both its claims of prejudice and its requested relief. Each of VLSI's supplemental damages contentions, including its most recent supplementation, have satisfied the requirements of PLR 3-8. Contrary to Intel's allegations, VLSI *has* provided computational details for its comparable licensing theory, as discussed in further detail below. It has identified the facts and factors that will be considered in VLSI's experts' analysis of whether the comparable royalty should be adjusted upwards or downwards to accommodate for differences with the hypothetical license. That VLSI's comparable-license contentions have not been linked to VLSI's overall \$5.4 billion damages claim ***for all six asserted patents*** is of no moment—VLSI has only proposed a comparable licensing methodology for a subset of patents, including the '836 Patent, and has applied that methodology on a per-patent basis. *See* Contentions at 81-87 (MicroUnity); 87-91 (WARF). And the *Georgia-Pacific* adjustments described above are the province of expert discovery.

Intel's motion is premature and unsupported by law; confuses the applicable legal standards; and improperly seeks to use its own discovery delays as both sword and shield. First, unlike infringement or invalidity contentions, *see* PLR 3-6, this Court does not require either party to seek leave in order to amend damages contentions. *See Looksmart Group, Inc. v. Microsoft Corp.*, 386 F. Supp. 3d 1222, 1232 (N.D. Cal. 2019). Intel's complaints that it "should have had the full discovery period to test and rebut VLSI's arguments" or that VLSI "under PLR 3-8 was

Intel Corp. v. Tela Innovations, Inc., 2021 WL 1222622, at *33 (N.D. Cal. 2021). Further, under settled Federal Circuit law, a plaintiff cannot introduce payment amounts of non-comparable agreements for any purpose. *Apple Inc. v. Wi-LAN Inc.*, 25 F.4th 960, 972 n.5 (Fed. Cir. 2022); *LaserDynamics, Inc. v. Quanta Computer, Inc.*, 694 F.3d 51, 80-81 (Fed. Cir. 2012).

required to disclose at the start of the case how any agreements it will rely on are comparable” run counter to the reasoning behind PLR 3-8. *Looksmart*, 386 F. Supp. 3d at 1230 (requiring no leave of court to amend damages contentions). Second, to the extent that Intel claims prejudice based on lack of discovery, any delay has been caused by Intel itself. Both Intel and VLSI disclosed damages theories based on *Intel’s* own past licenses (VLSI on December 12, 2018; and Intel on September 7, 2018), but Intel only agreed to search for documents for its *own* comparable licenses. Intel has *still* not produced negotiation materials for VLSI’s comparable agreements. Thus, only *Intel* is in possession of any discovery that remains outstanding.

All three categories of relief sought by Intel’s motion should be denied:

1. **Intel’s agreements with WARF and MicroUnity:** VLSI’s comparable licensing theories are neither deficient nor untimely, and should not be precluded.
2. **Intel’s agreements with DEC, Intergraph, [REDACTED] NVIDIA, [REDACTED] and Transmeta:** VLSI has not offered comparable license theories for these agreements and should not be precluded from relying on agreements for rebuttal purposes before expert discovery even begins; this dispute is not ripe for adjudication.
3. **All patent agreements for any reason:** Intel seeks discovery sanctions and an advisory opinion on the admissibility of allegedly “non-comparable” agreements—both requests are speculative, premature, and lack any legal basis.

1. VLSI’s WARF and MicroUnity Analyses Are Timely And Sufficient Under PLR 3-8

VLSI’s supplementation on the WARF and MicroUnity licenses complies with both PLR 3-8 and this Court’s October 2018 Order. The law of this district requires supplementation of damages contentions when a party’s damages theory “shifts in some material respect.” *Looksmart*, 386 F. Supp. 3d at 1227. VLSI supplemented its damages contentions three times in response to material shifts in its theories, this time to include more details for its incremental benefit damages theory (not at issue in Intel’s motion), and additional licensing theories for Intel’s \$110 million agreement with WARF and its \$300 million agreement with MicroUnity.

VLSI’s disclosures are not deficient. VLSI disclosed extensive factual details underlying its experts’ anticipated *Georgia-Pacific* analysis (including all attendant technological and economic comparability considerations). *See* Contentions at 80-91. Intel contends that VLSI “still has not connected” the WARF and MicroUnity agreements “to its extraordinary \$5.4 billion damages demand,” but ignores that the \$5.4 billion number covers *all* asserted patents, whereas VLSI’s comparable-license contentions for WARF and MicroUnity will be applied on a per-patent basis.

Intel’s motion also ignores that a comparability theory requires *expert analysis* to establish comparability, and to adjust the comparable royalty rate based on upward, downward, and neutral adjustments. *See generally Ericsson, Inc. v. D-Link Sys., Inc.*, 773 F.3d 1201, 1227 (Fed. Cir. 2014). In its Fourth Amended Damages Contentions, VLSI identified comparable licenses, and set forth specific facts and categories of evidence that its experts may consider in their comparability *and Georgia Pacific* analyses. Contentions at 85-87; 89-91. This comparability analysis could yield a damages number different from the damages number associated with VLSI’s incremental benefit analysis. But the precise calculation will depend on the extent of infringement along with other, standard, *Georgia-Pacific* adjustments that will ultimately be addressed and determined by VLSI’s experts in their expert reports.

The only thing VLSI has **not** disclosed is the expert analysis itself, which is not due until March 22, 2023. Intel's motion to strike VLSI's WARF and MicroUnity analyses should be denied.

2. Intel's Request To Strike VLSI's Rebuttal Evidence Is Premature

As to the remainder of the Intel agreements that VLSI disclosed in December 2018, including the DEC, Intergraph, [REDACTED] NVIDIA, [REDACTED] and Transmeta agreements, VLSI has proffered those agreements only **for rebuttal** to comparable licensing theories that may be advanced by Intel's experts. Intel's motion is premature and should be denied.

Intel argues that the agreements should be stricken because "the Court's Order did not contain any [rebuttal] exception," and VLSI has not disclosed "how any agreements it will rely on are comparable and allegedly support its damages number." But VLSI has not offered these Intel agreements in support of its damages number. VLSI has only offered the agreements, out of an abundance of caution, as *potential* rebuttal evidence to Intel's damages theories,³ including because Intel has disclosed that it *may* offer a comparable licensing analysis based on a subset of Intel licenses for amounts ranging from \$140,000 to \$15 million, and that it *may* refer to "evidence" of Intel's licensing practices. VLSI has thus disclosed that it *may* offer, in rebuttal, Intel agreements carrying from [REDACTED] to "shed light" on Intel's *actual* licensing practices. *Tela Innovations*, 2021 WL 1222622, at *33. At least one plaintiff has been allowed to provide that type of rebuttal in this District.⁴

Because it would be premature to analyze the sufficiency of VLSI's rebuttal disclosures before expert discovery, Intel's motion should be denied.

3. Intel Identifies No Basis To Preclude VLSI From Relying On All Patent Agreements

Intel seeks an "an order precluding VLSI from relying on **any patent agreements in this case**," but offers no basis and cites no caselaw that would support the extraordinary sanction of evidentiary preclusion. In the only case in which this District has levied evidentiary sanctions based on PLR 3-8, a plaintiff was merely precluded from relying on **specific new facts** that were disclosed one month **after** the close of discovery. *See Netfuel, Inc. v. Cisco Sys. Inc.*, 2020 WL 4381768, at *6 (N.D. Cal. July 31, 2020). Intel's only cited case sanctioned a plaintiff that outright **refused to amend** its PLR 3-1 infringement contentions because it would be "too expensive." *Shared Memory Graphics LLC v. Apple Inc.*, 2011 WL 3878388 (N.D. Cal. Sept. 2, 2011). In contrast, VLSI has expended hundreds of attorney and expert hours investigating and amending all of its PLR contentions. And unlike PLR 3-8, PLR 3-1 has a timeliness requirement requiring good cause and leave to amend. Intel's case is not only factually distinguishable—it is the wrong law altogether.

VLSI respectfully submits that the Court should deny all of Intel's requested relief.

³ *Tela Innovations*, 2021 WL 1222622, at *33 ("[This case] is unlike Intel's leading case, *Lucent Technologies., Inc. v. Gateway, Inc.*, 580 F.3d 1301 (Fed. Cir. 2009), for several reasons, including that the Federal Circuit there was reviewing a damages award based on sufficiency of the evidence and the non-comparable agreements were proffered as the evidence to support the award.").

⁴ As this District has recognized, the Federal Circuit has **not** ruled on the admissibility of non-comparable agreements outside the context of an affirmative *Georgia-Pacific* analysis. *See, e.g., Tela Innovations, Inc.*, No. , 2021 WL 1222622, at *33 (allowing plaintiff's expert to opine on "several previous licenses involving Intel with large lump sum payments up to \$1.5 billion" "to shed light on Intel's general licensing practices, including its purported willingness to make 'significant lump sum payments where it recognizes infringement risks'").

Dated: December 2, 2022

By: /s/ Charlotte J. Wen
Charlotte J. Wen

IRELL & MANELLA LLP

Morgan Chu (SBN 70446)
Benjamin W. Hattenbach (SBN 186455)
Amy E. Proctor (SBN 283845)
Dominik Slusarczyk (SBN 287084)
Charlotte J. Wen (SBN 313572)
1800 Avenue of the Stars, Suite 900
Los Angeles, California 90067-4276
Telephone: (310) 277-1010
Facsimile: (310) 203-7199
Email: mchu@irell.com
Email: bhattenbach@irell.com
Email: aproctor@irell.com
Email: dslusarczyk@irell.com
Email: cwen@irell.com

Counsel for Plaintiff
VLSI TECHNOLOGY LLC

Respectfully submitted,

By: /s/ Mark D. Selwyn
Mark D. Selwyn

**WILMER CUTLER PICKERING
HALE AND DORR LLP**

William F. Lee (*pro hac vice*)
william.lee@wilmerhale.com
Louis W. Tompros (*pro hac vice*)
louis.tompros@wilmerhale.com
Dominic E. Massa (*pro hac vice*)
dominic.massa@wilmerhale.com
60 State Street
Boston, MA 02109
Telephone: (617) 526-6000
Fax: (617) 526-5000

**WILMER CUTLER PICKERING
HALE AND DORR LLP**

Mark D. Selwyn (SBN 244180)
mark.selwyn@wilmerhale.com
2600 El Camino Real, Suite 400
Palo Alto, CA 94306
Telephone: (650) 858-6000
Fax: (650) 858-6100

**WILMER CUTLER PICKERING
HALE AND DORR LLP**

Amanda L. Major (*pro hac vice*)
amanda.major@wilmerhale.com
1875 Pennsylvania Avenue NW
Washington, DC 20006
Telephone: (202) 663-6000
Fax: (202) 663-6363

Attorneys for Defendant
INTEL CORPORATION